FLAG-ERA ***Kick-off meeting***

Project **GraNitE:**

Graphene heterostructures with Nitrides for high frequency Electronics

Filippo Giannazzo

Consiglio Nazionale delle Ricerche (CNR),
Institute for Microelectronics and Microsystems (IMM),
Catania, Italy

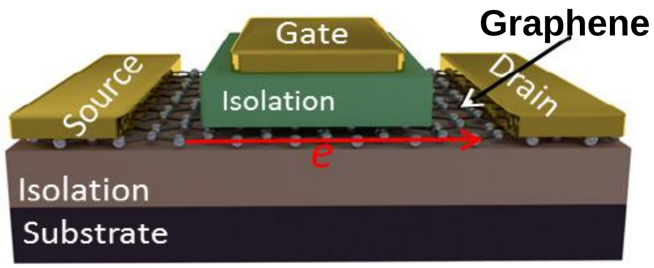
Outline

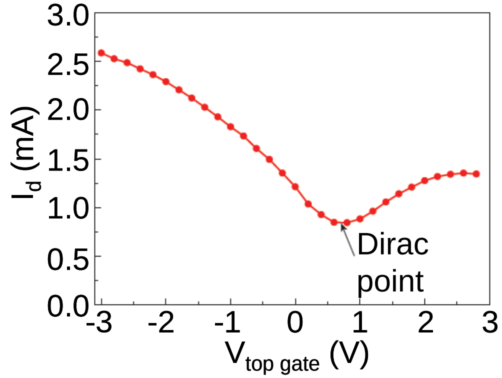
- **Description of the project and research method:**
  - *State of the art*
  - *Objectives*
  - *Consortium*
  - *Implementation, workplan*

- **Interaction with the Graphene Flagship Core1 project**

- **Expected impacts**

Lateral graphene field effect transistors (GFETs)





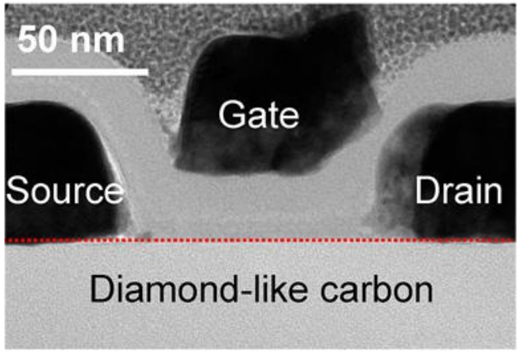
$I_{on}/I_{off}<10$

high I_{off} **Power dissipation**

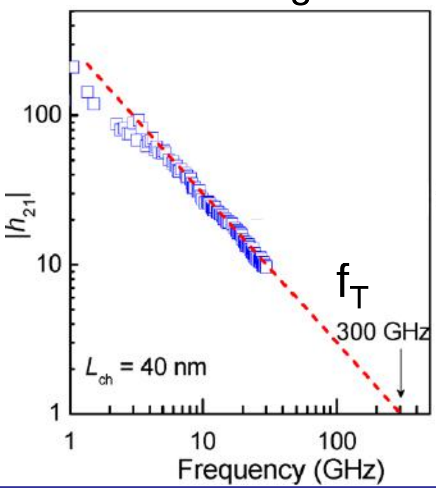
No bandgap in Gr banstructure

State of the art RF transistors

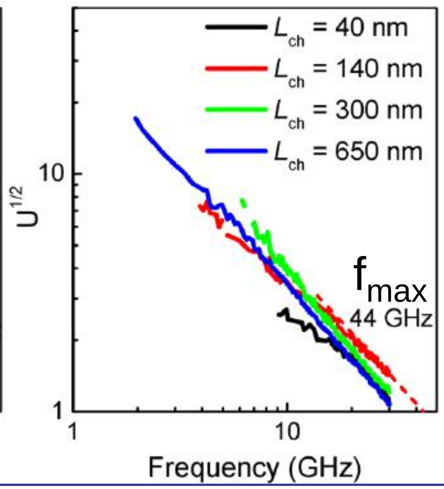
CVD graphene



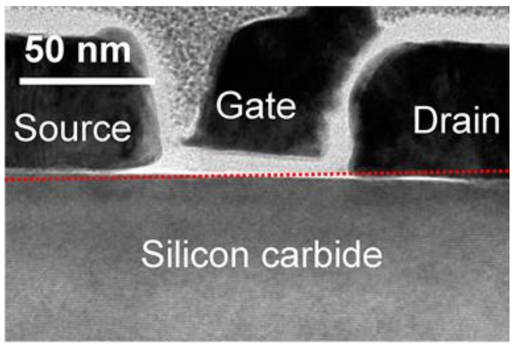
Current gain



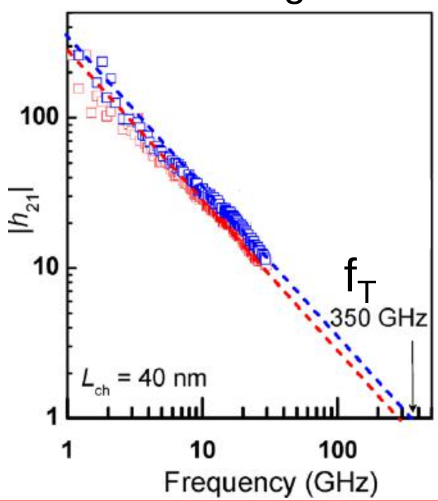
Power gain



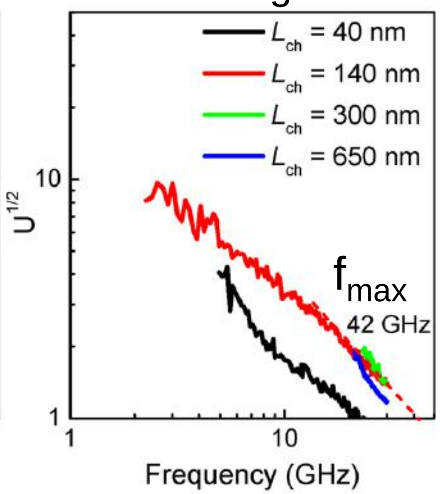
Epitaxial graphene on SiC

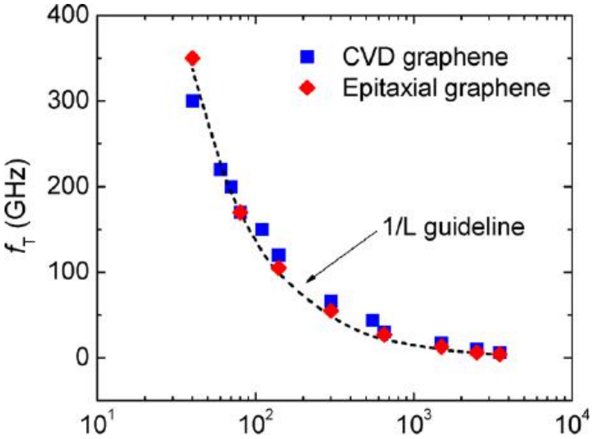


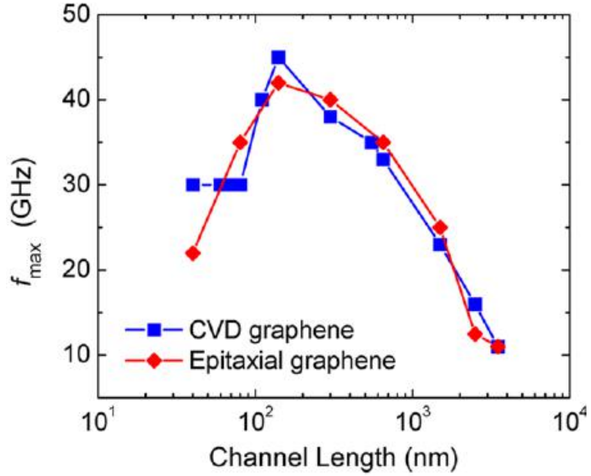
Current gain



Power gain



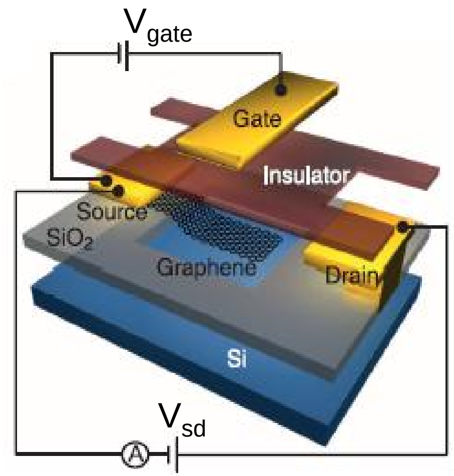


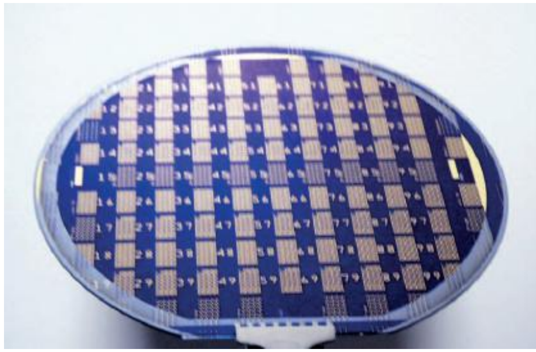


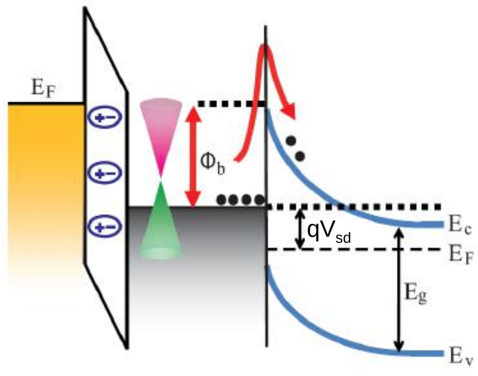
Y. Wu, et al, Nano Lett., 12, 3062−3067 (2012).

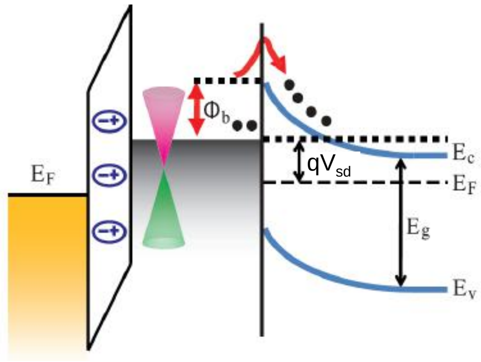
Graphene integration with semiconductors technology

Graphene/Si Schottky diode with gate modulated barrier height: Barristor

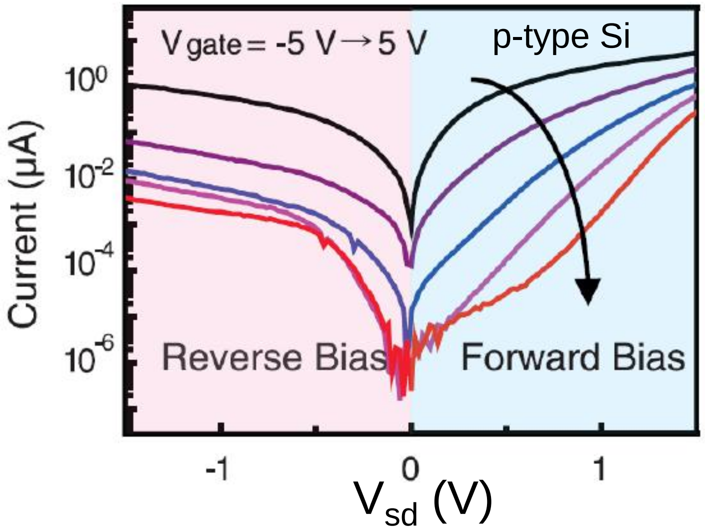




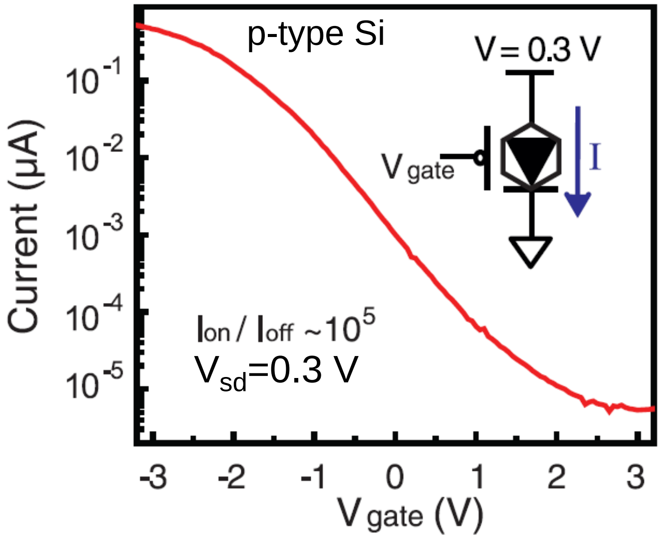




Output characteristics

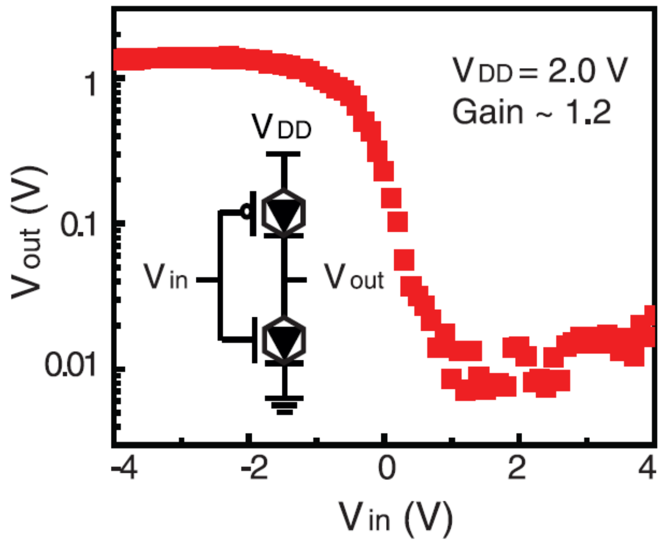


Transfer characteristics



Applications

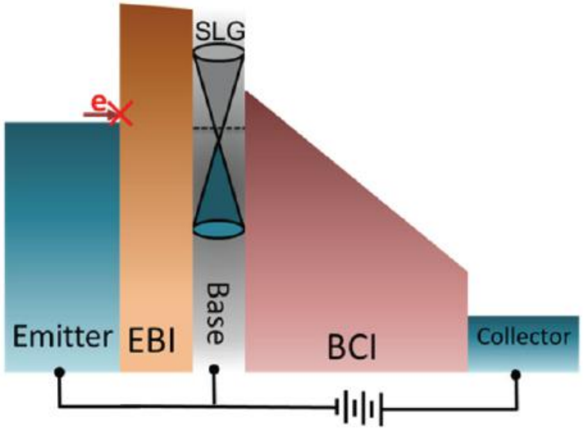
Logic circuits: inverter

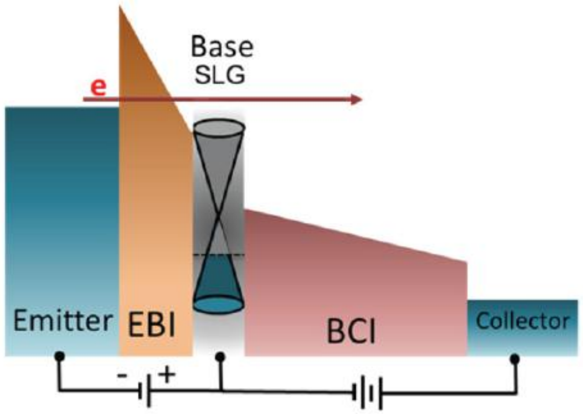


H. Yang, J. Heo, S. Park, H. Jae Song, D. H. Seo, K.-E. Byun, P. Kim, I. Yoo, H.-J. Chung, K. Kim, Science 336, 1140- 1143 (2012)

Graphene integration with semiconductor technology

Hot electron transistor (HET) with a graphene base



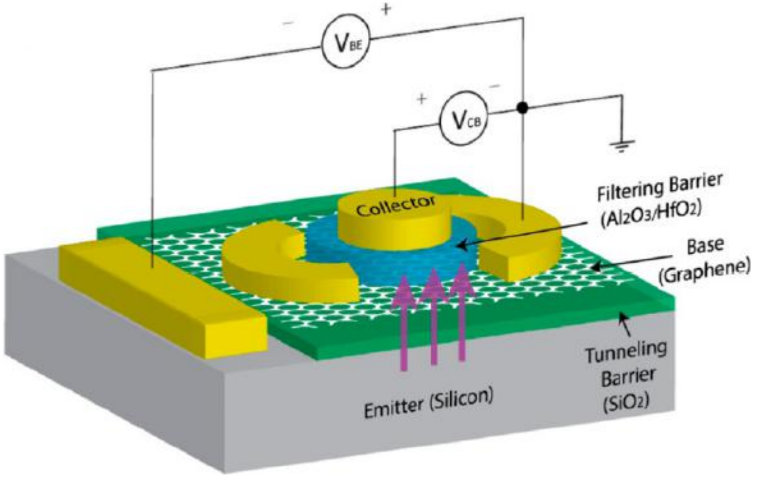


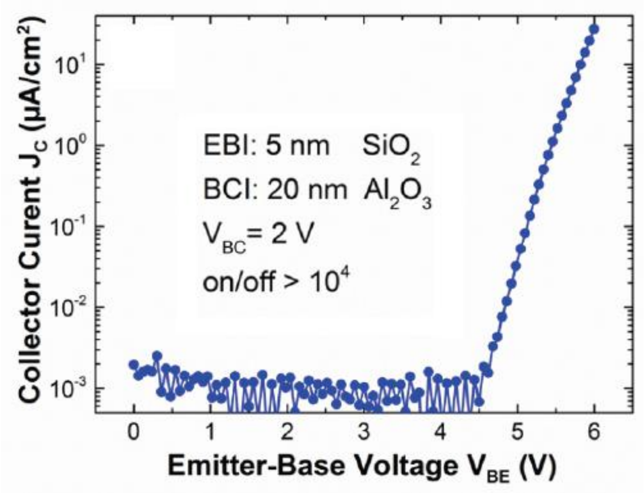
-Current injection of from the emitter into the Gr base by Fowler-Nordheim (FN) tunneling controlled by V_{BE}.

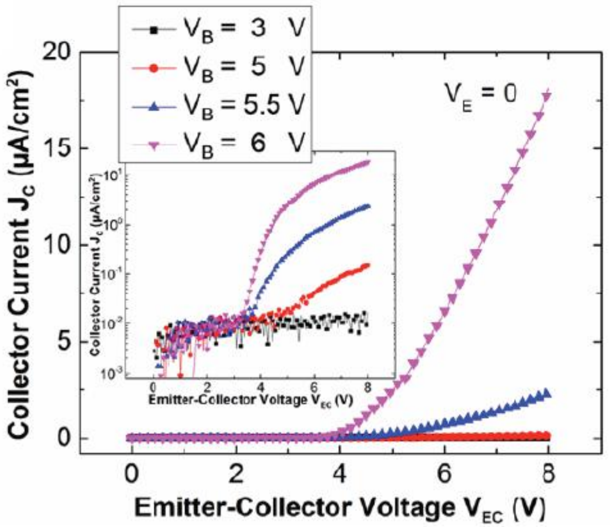
- Injected electrons ballistically transit in the Gr base.
- After overcoming a filtering barrier layer, hot electrons are collected at the collector terminal.

Graphene ideal material for the base of HET → THz operation predicted

State of the art graphene HETs







C. Zeng, E. B. Song, M. Wang, S. Lee, C. M. Torres, J. Tang, B. H. Weiller, K. L. Wang, Nano Lett. 13, 2370−2375 (2013)

S. Vaziri, G. Lupina, C. Henkel, A. D. Smith, M. Ostling, J. Dabrowski, G. Lippert, W. Mehr, M. C. Lemme, *Nano Lett.* **13**, 1435 (2013)

Graphene integration with group III-Nitride (III-N) semiconductors

Motivations: GaN material of choice for optoelectronics (LED, lasers)…
….and energy efficient high frequency electronics

I. Akasaki H. Amano S. Nakamura

for the invention of efficient blue light-emitting diodes which has enabled bright and energy-saving white light sources

	Si	GaN
Bandgap (eV)	1.11 (Indirect)	3.4 (Direct)
Intrinsic carrier concentration (cm^{-3}) at 300 K	1.5×10^{10}	1.9×10^{-10}
Electron mobility ($cm^2V^{-1}s^{-1}$)	1350	1600
Saturation electron velocity (10^7 cm/s)	1.0	2.7
Critical electric field (MV/cm)	0.3	3.3
Thermal conductivity (W/cmK)	1.5	2.1

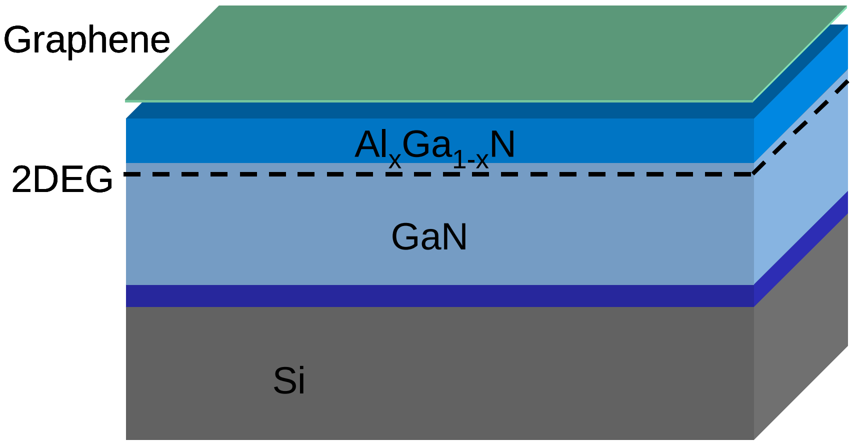
Very low off-state currents

Superior current transport

Higher breakdown voltage

Superior heat dissipation

Large area system of electrostatically coupled Dirac and Schroedinger 2DEGs

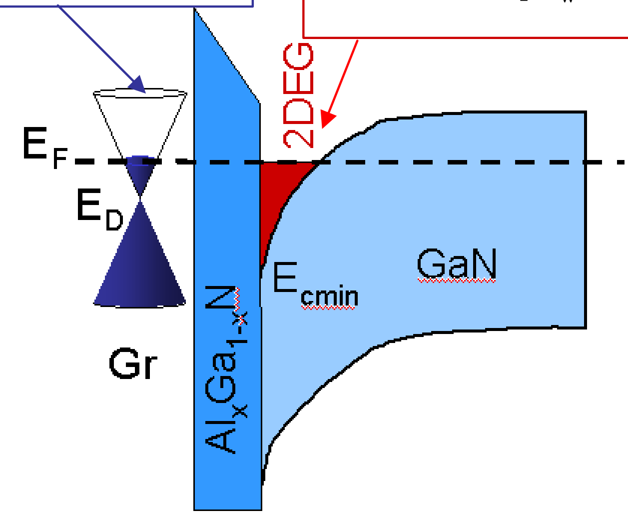


Dirac electrons

$$E_F - E_D = \frac{\hbar v_F \sqrt{\pi n_{gr}}}{q}$$

Schroedinger electrons

$$E_F - E_{c\,min} = \frac{\pi\hbar^2}{q m_w^*} n_s + \frac{1}{q}\left(\frac{9\pi\hbar q^2}{8\varepsilon_0\varepsilon_{AlGaN}\sqrt{8m_w^*}}\right)^{\frac{2}{3}} n_s^{\frac{2}{3}}$$



GraNitE: Graphene heterostructures with Nitrides for high frequency Electronics

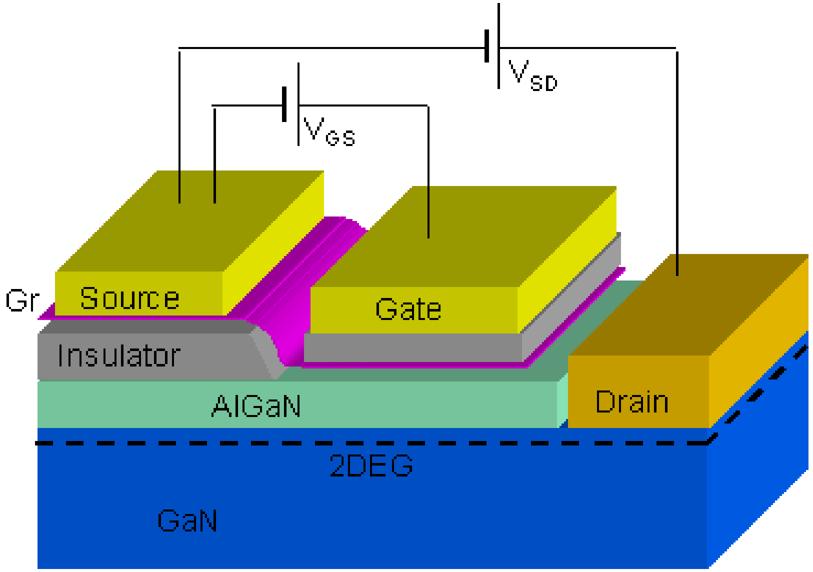
Objectives:

(i) Design, fabrication, structural and electrical characterization of **high quality graphene (Gr) heterostructures with thin films of Nitrides**, i.e. GaN, AlN and related alloys ($Al_xGa_{1-x}N$).

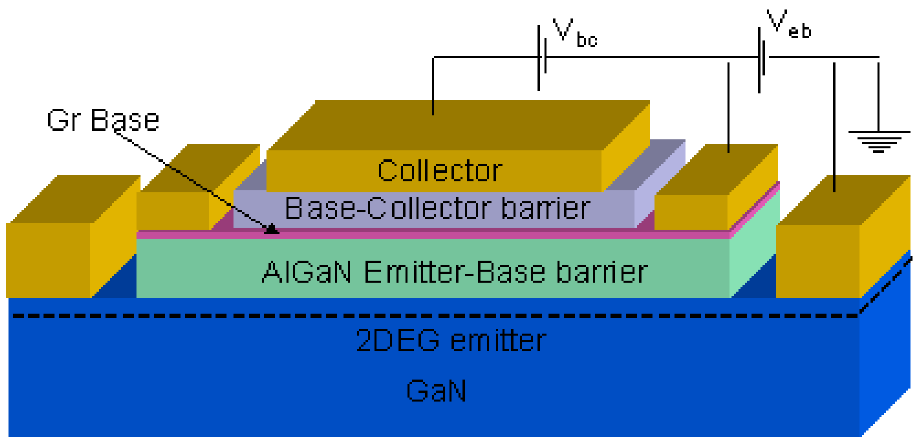
- III-N layers grown by MBE or MOCVD on different substrates: Al_2O_3, SiC, GaN, Si.
- **Transfer** of CVD grown Gr from Copper to III-N or **direct growth** of Gr on III-N and of III-N on Gr.
- Advanced structural and electrical characterization of the heterostructures: understanding current transport mechanisms at the interfaces.
- Multiscale simulations for the growth, processing and device design.

(ii) Demonstration of novel device structures

Graphene/AlGaN/GaN *Schottky diode with a gate modulated Schottky barrier (**Barristor**) for logic applications*



Graphene *Base-Hot Electron Transistor* (GB-HET) on Nitride heterostructures for ultrahigh frequency (THz) applications



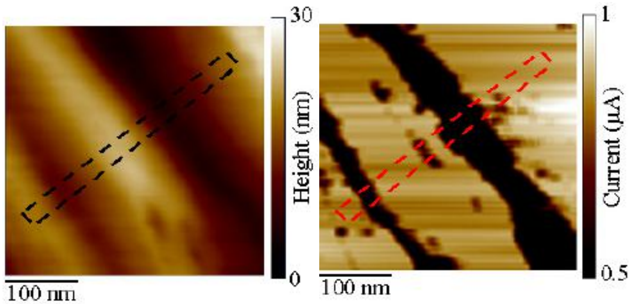
GraNitE project's consortium

IMM
Catania, Italy

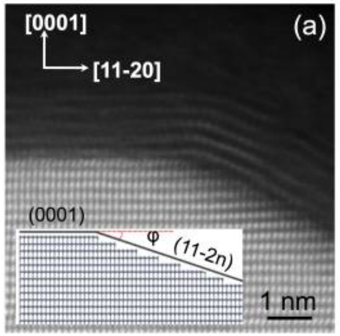
PI: *F. Giannazzo*, ***Co-PIs:*** *F. Roccaforte, A. La Magna*

Advanced characterizations

SPM



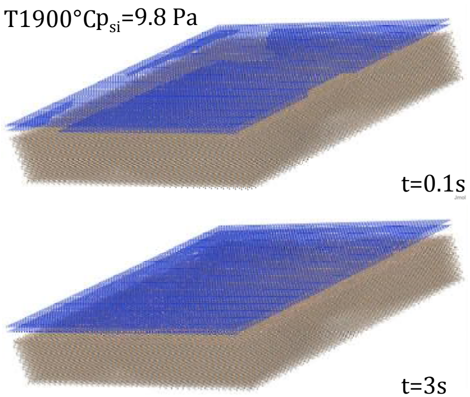
Atomic resolution STEM



G. Nicotra, Q. M. Ramasse, I. Deretzis, A. La Magna, C. Spinella, F. Giannazzo, ACS Nano 7, 3045 (2013)

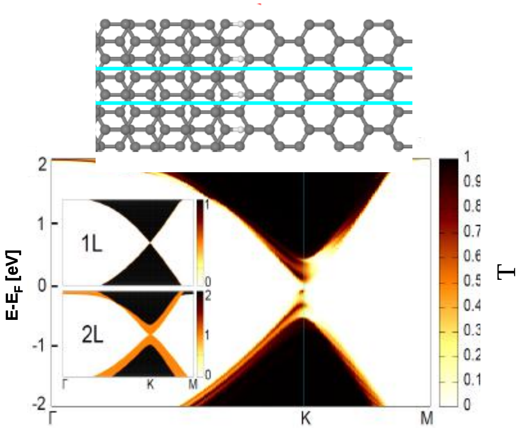
Multiscale simulations

Process simulations
Example: epitaxial graphene growth



I. Deretzis et al., Phys. Rev. E 93, 033304 (2016)

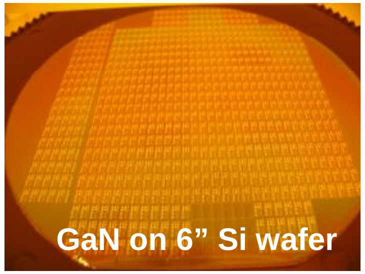
Electronic transport simulations

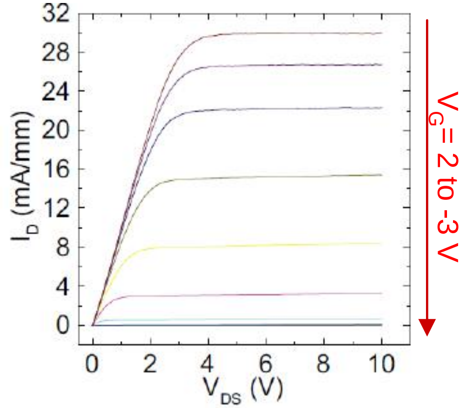


F. Giannazzo, et al., Phys Rev. B **86**, 235422 (2012)

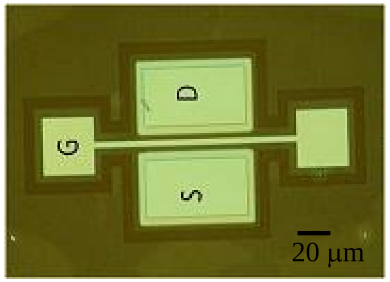
Processing and devices prototyping

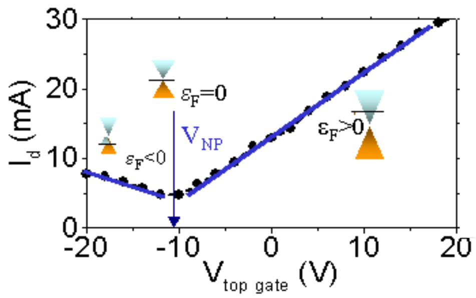
GaN-based HEMTs

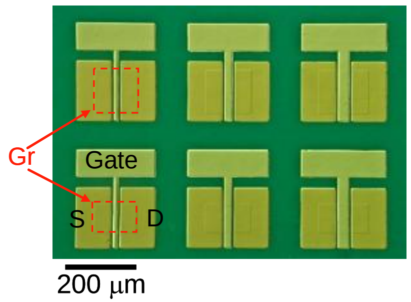


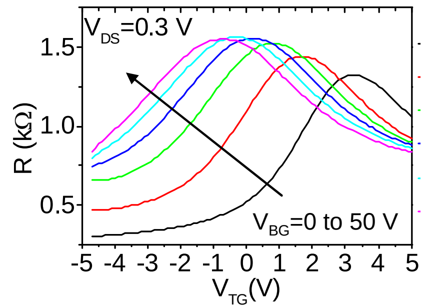


Graphene field effect transistors









GraNitE project's consortium

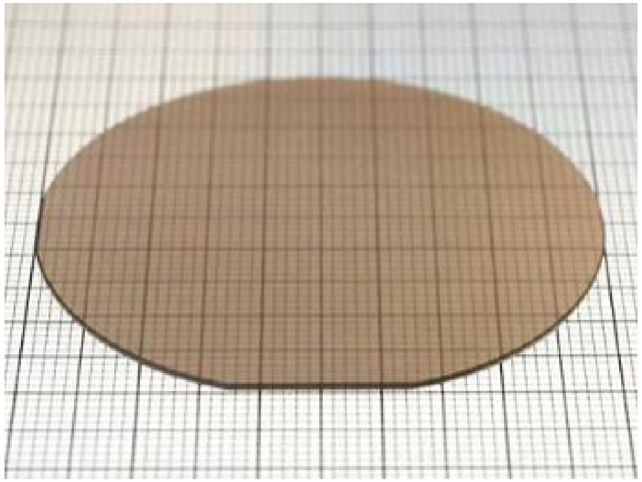
TopGaN

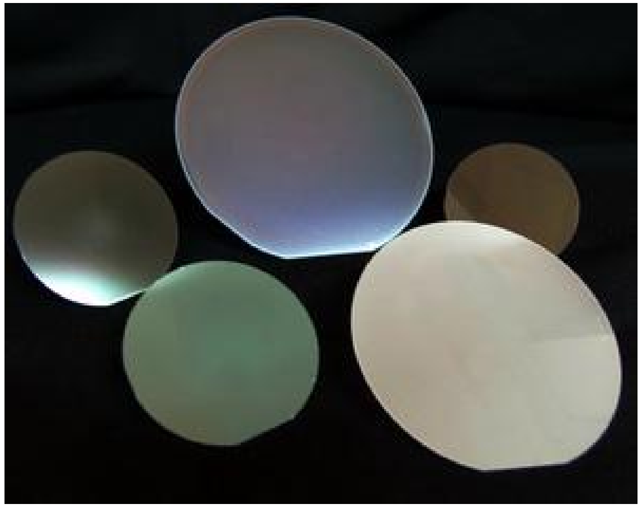
Warsaw, Poland

PI: *M. Leszczyński*, ***Co-PIs:*** *P. Kruszewski, P. Prystawko*

Growth of III-N epi structures on different substrates: Al_2O_3, SiC, bulk-GaN

Technology for GaN-based power devices, LEDs, Lasers



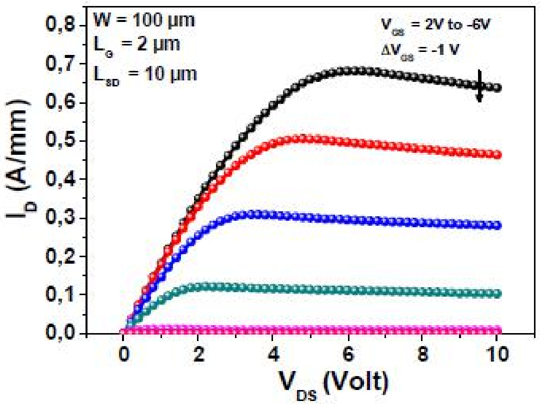


GraNitE project's consortium

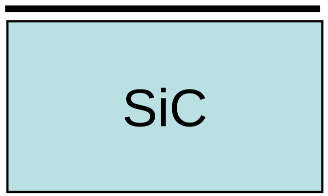
CNRS CRHEA
Valbonne, France

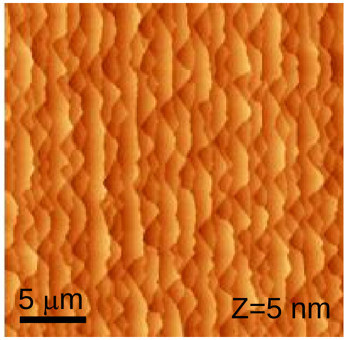
PI: *Y. Cordier*, ***Co-PI:*** *A. Michon, E. Frayssinet*

MOCVD growth of III-N multilayers on silicon wafers (up to 150 mm)



CVD growth of Gr on SiC

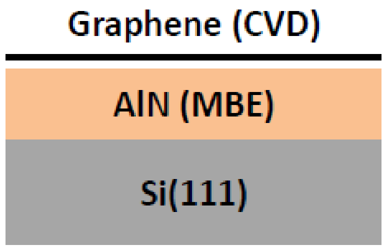


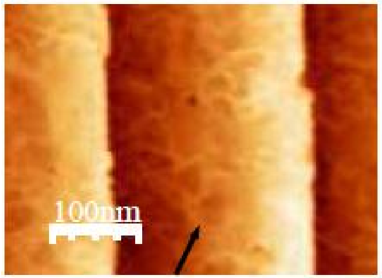


$n_s = 1.8 \times 10^{11}$ cm^{-2}
$\mu = 9400$ cm^{2}V^{-1}s^{-1}

R. Ribeiro-Palau et al., Nature Nanotechnology 10, 965 (2015)

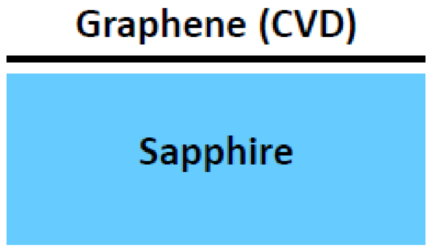
CVD growth of Gr on AlN thin films on Si

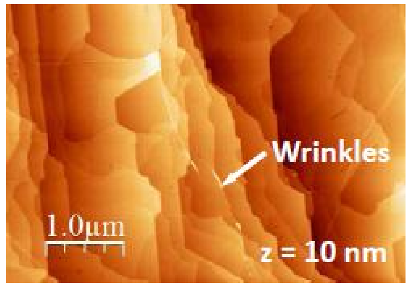




Wrinkles and small domains

CVD growth of Gr on Al_2O_3 (sapphire)





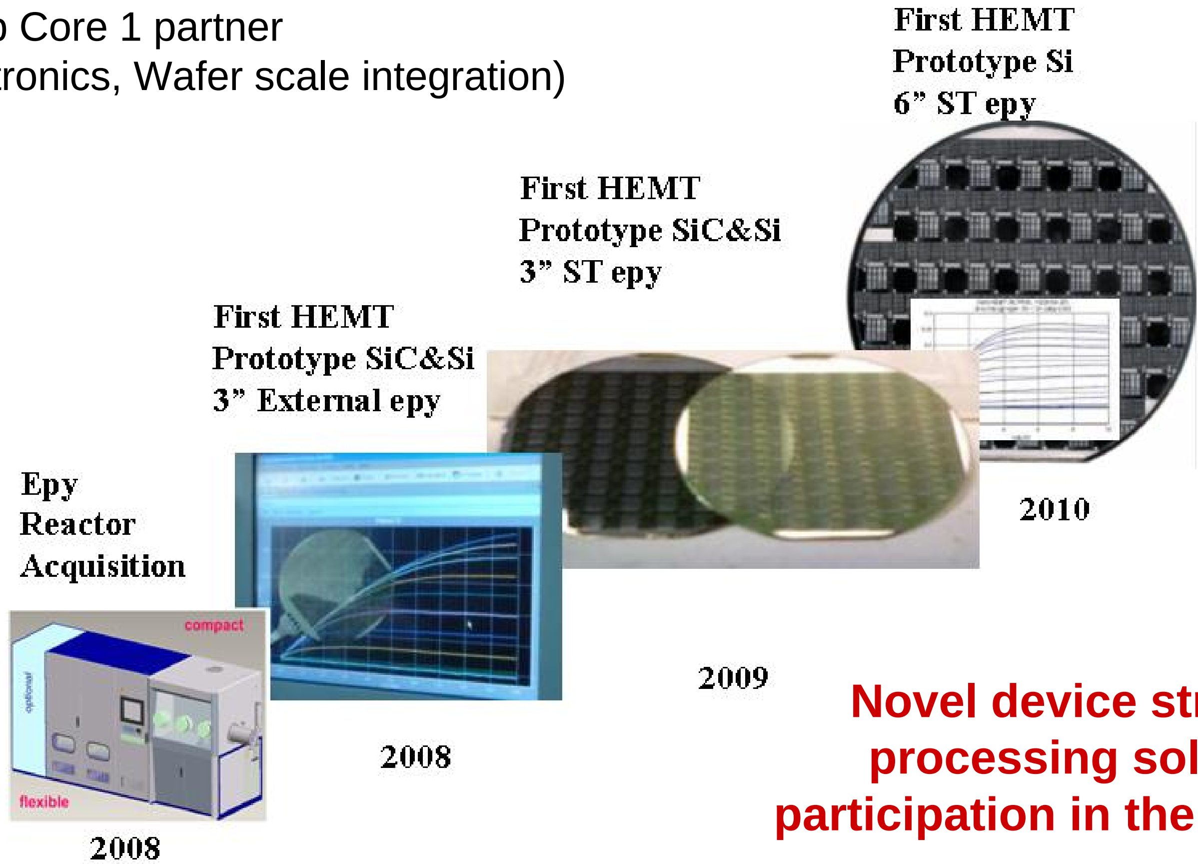
A. Michon, et al., APL **104**, 071912 (2014).

GraNitE project's consortium

Catania, Italy

PI: *S. Ravesi*, ***Co-PIs:*** *F. Iucolano, S. Lo Verso*

- One of the largest microelectronics industries in Europe
- Strong commitment in GaN technology for energy efficient power and high frequency electronics
- GaN pilot line in the Catania site
- Graphene Flagship Core 1 partner
  (WPs Flexible electronics, Wafer scale integration)



Novel device structures and processing solutions from participation in the GraNitE project

GraNitE project's consortium — Roles of the partners

CNR IMM

-Project coordination,
-Processing
-Characterizations,
-Simulations

- Key process steps: Gr transfer, 2DEG isolation, ALD deposition of dielectrics, contacts,..
- Device design and multiscale simulations
- Fabrication of device test structures and prototypes
- Advanced structural/electrical characterizations (SPM, TEM).

TopGaN

-Growth of Nitride Substrates/multilayers
- Characterizations

- Growth of AlGaN/GaN on different substrates: Al_2O_3, SiC, bulk-GaN
- Characterization (AFM, XRD, CV) of as-grown epi-wafers

CNRS CRHEA

-Growth of Graphene/Nitrides heterostructures
-Characterizations

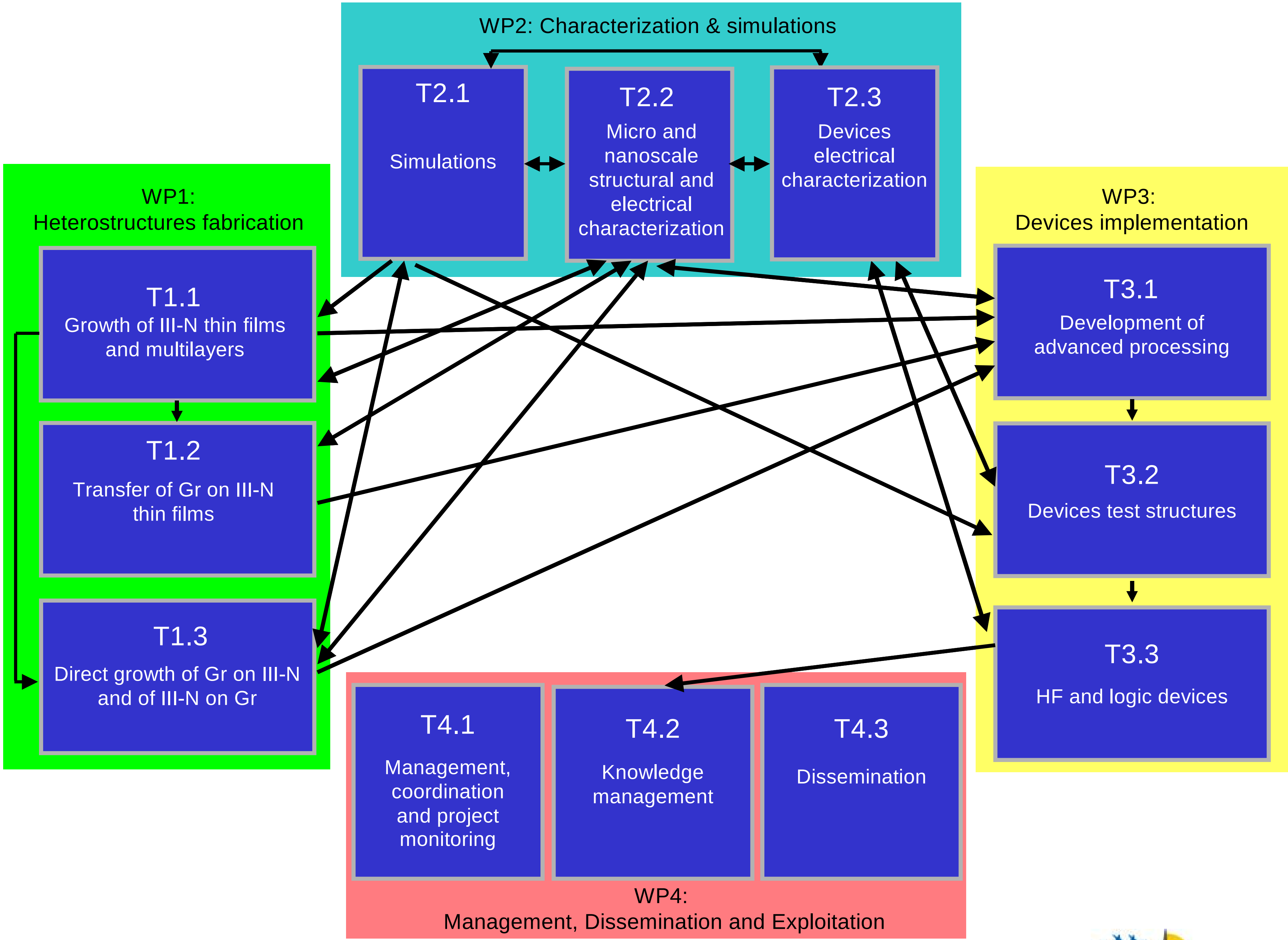
- Growth of AlGaN/GaN on 6" Si wafers
- CVD growth of Gr on III-N thin films
- MOCVD growth of III-N thin films on Gr
- Characterization (LEED, XPS, AFM, SEM, XRD) of as grown heterostructures

ST life.augmented

Device processing in a semiconductor fab environment

- Processing of Gr/AlGaN/GaN heterostructures on 6" silicon wafers
- Testing of high frequency devices.
- Exploitation management

Project’s implementation



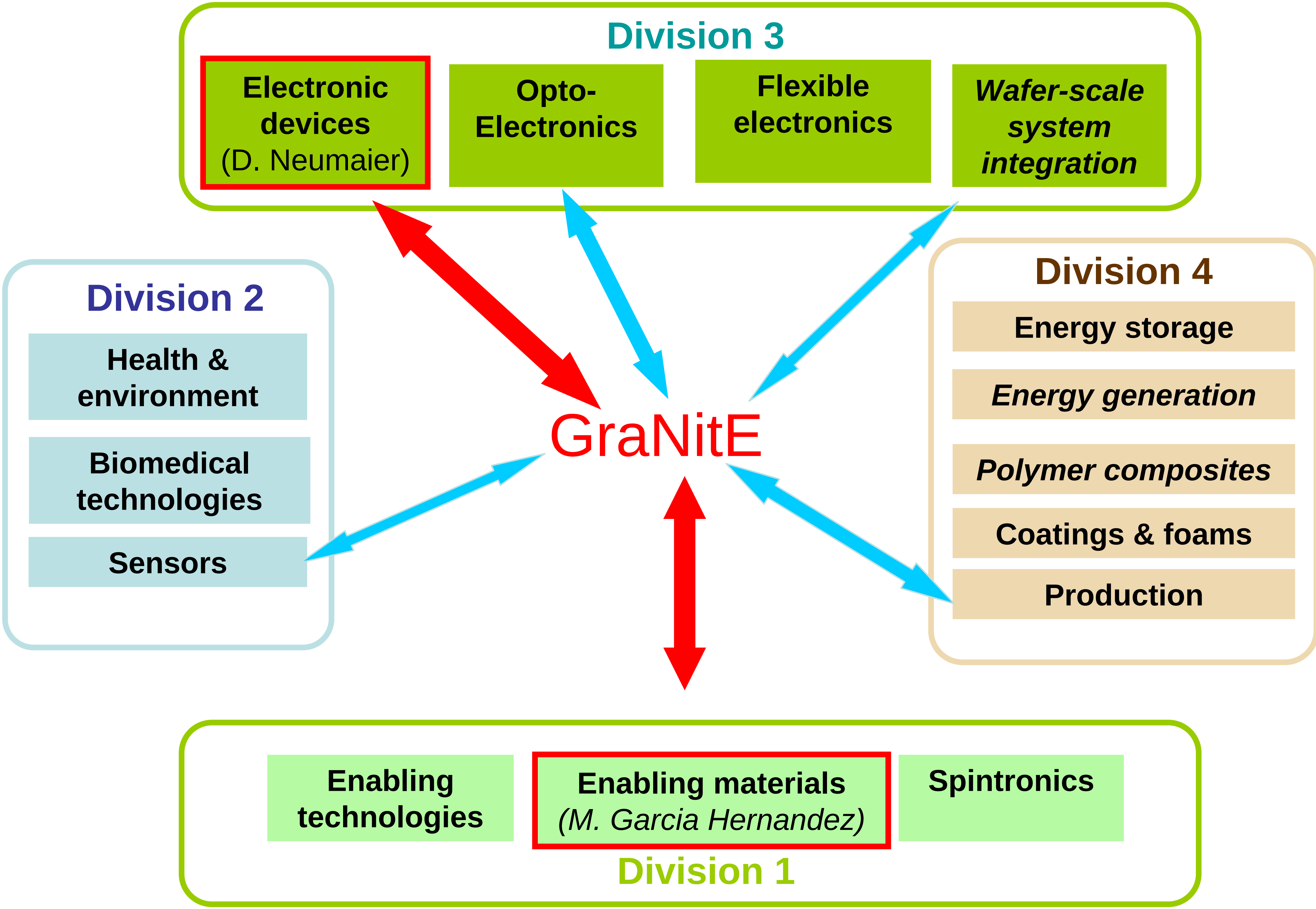
Project's implementation

Gannt Chart

WP	Task		Partners	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
				First Year												Second Year												Third Year											
WP 1 Heterostructures fabrication	T1.1	Growth of III-N thin films and multilayers	**TopGaN**,CNRS,CNR												D1.1																								
	T1.2	Transfer of Gr on III-N thin films	**CNR**, STM																D1.2																				
	T1.3	Direct growth of Gr on III-N and of III-N on Gr	**CNRS**, TopGaN, CNR																		D1.3						D1.4 M2												
WP2 Characterization and simulations	T2.1	Simulations	**CNR**,TopGaN,CNRS						D2.1								D2.3														D2.5				D2.7				
	T2.2	Nanoscale structural and electrical characterization	**CNR**,TopGaN,CNRS														D2.2						D2.4																
	T2.3	Devices electrical characterization	**CNR**, STM																										M3				D2.6						D2.8
WP3 Devices implementation	T3.1	Development of advanced processing	**CNR**, STM, TopGaN																								D3.3												
	T3.2	Device test structures	**CNR**, STM											D3.1																	D3.4								
	T3.3	HF and logic devices	**STM**, CNR																				D3.2								M4						D3.5		
WP4 Management, Dissem. & Expl.	T3.1	Management, coordination and project monitoring	**CNR**, TopGaN, CNRS, STM												D4.2												D4.3												D4.4
	T3.2	Knowledge management	**STM**, CNR															M1																					
	T3.3	Dissemination	**CNR**, CNRS						D4.1																														

- Starting date: February 1, 2016
- Kick-off meeting: Catania, February 25, 2016

Interactions with the Graphene Flagship Core 1 project



Interactions with the Graphene Flagship Core 1 project

GraNitE project's activity

Development of large area and high quality Gr heterostructures with III-N thin films:
-Gr transfer from Cu to III-N layers
- CVD growth of Gr on III-N and of III-N thin films on Gr.

Novel electronic devices based on Gr heterostructures with AlGaN/GaN junctions hosting a 2DEG at the interface:
- *Gr/semiconductor Schottky diode with a gate modulated Schottky barrier*
- *Gr Base Hot Electron Transistor*

Graphene Flagship Core 1 WP

Enabling materials *(M. Garcia Hernandez)*
- Synergies with the groups working on the large area growth of Gr on SiC (e.g. Linkoping University) and on metals.
- Interactions with the characterization and modelling groups.

Electronic devices *(D. Neumaier)*
- Comparison with other device schemes developed using different heterostructures for benchmarking.
- Interactions with the groups working on devices simulations and high frequency electrical characterization

GRAPHENE FLAGSHIP

Memorandum of Understanding (MoU)

for association of a Partnering Project to the Graphene Flagship

Following the submitted application and the approval by the Graphene Flagship Executive Board/Management Panel, the project:

GRAPHENE HETEROSTRUCTURES WITH NITRIDES FOR HIGH FREQUENCY ELECTRONICS (GRANITE)

becomes associated to the Graphene Flagship initiative as a Partnering Project (PP).

On behalf of the Graphene Flagship Core 1 Project:

WP Electronic devices or WP Enabling Materials Leader or Deputy
Name and signature:
Daniel Neumaier

On behalf of the Partnering Project:

PP coordinator
Name and signature:
Filippo Giannazzo

Interactions with other FlagERA JTC2015 projects

Linkoping University, Sweden

A. Kakanakova, R. Yakimova, G. K. Gueorguiev, V. Khranovsky

GRIFONE:
Graphitic films of group III nitrides and group II oxides: platform for fundamental studies and applications

IMM, Catania

P. Fiorenza, F. Giannazzo

Hungary

B. Pécz, J. Lábár, L. Tóth

Expected impacts

Development of hybrid Graphene/III-N technology :
know-how on materials, processing, devices

Significant scientific and technological impacts in important areas of ICT and beyond

***High-frequency electronics*:**
Vertical hot electron transistors based on graphene/AlGaN/GaN heterostructures with cut-off frequency f_t>1THz, common base current gain α>1, collector current density up to J_c>1A/cm^2.

***New logic devices*.**
Gate modulated Gr/AlGaN/GaN Schottky *diodes (Barristors) with* I_{on}/I_{off}>10^8, very low I_{off}<10_{-12} A (i.e. very low power dissipation) and the possibility to operate at temperatures >200 °C (applications in special environment).

***Production of Gr/III-N heterostructures on large area*.**
High quality heterostructures of Gr with III-N thin films/multilayers grown on different substrates including Si (6 inches wafers), SiC, Sapphire, GaN (from 1 to 3 inches wafers).

Potential applications in several fields: optoelectronics (LEDs, lasers), sensing,…

In line with the objectives of Graphene Flagship:
Transformational impact on science and technology and substantial benefits for the European economy and society.

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